Performance Evaluation of a Symbol Synchronizer for OFDM Systems under Multi-path Environment

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Abstract

In this paper, we propose an improved symbol synchronizer applicable to OFDM packet communications. The performance of the synchronizer is evaluated in terms of false detection probability in the presence of additive white Gaussian noise (AWGN) and multi-path.

1. INTRODUCTION

The multi-carrier communication systems utilizing the Orthogonal Frequency Division Multiplex (OFDM) scheme are considered to be promising for providing broadband multimedia communications. In these systems, it is necessary to synchronize the timing for Fast Fourier Transform (FFT), called the symbol synchronization, at the receive end. In this paper, we propose an improved symbol synchronizer applicable to OFDM packet communications. This symbol synchronizer performs based on the envelope detection without a necessity for carrier recovery. The synchronization is established through the processing such as FFT, correlation, selection for the maximum correlated output, and accumulation. The basic performance of in terms of the false detection probability of the symbol synchronizer is evaluated in the presence of additive white Gaussian noise (AWGN) and multi-path through computer simulations.

2. SYSTEM DESCRIPTION

2.1. Transmit circuit

A generic configuration of transmit circuit for OFDM signals is shown in Fig.1. For conventional OFDM signals, for example, d is always "1" and information data are carried on the sequence $\{c(0),c(1)\ldots c(L\text{-}1)\}$. For multi-carrier spread-spectrum signals, on the other hand, the binary input data d are applied and divided into L parallel streams, each of which is multiplied by each element (chip) of spreading code sequence $\{c(0),c(1)\ldots c(L\text{-}1)\}$.

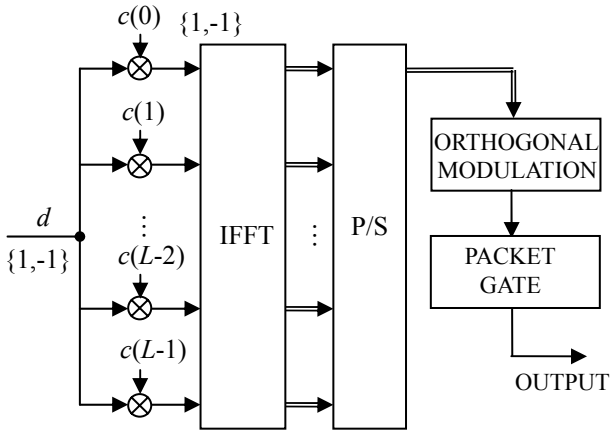


Fig.1. Transmit circuit

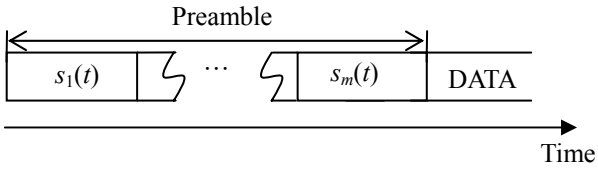


Fig.2. Packet composition

Prior to the data potion, a preamble is added for achieving the symbol synchronization at the receive end. For the preamble, several symbols of code sequences with the same pattern are generated, that is, d is always "1" and the code sequence $\{c(0),c(1)\ldots c(L\text{-}1)\}$ is also of a fixed

pattern. Figure 2 shows an example of packet format consisting of the preamble and the data portions.

The length of preamble is decided according to the number of accumulation in the accumulator described later. We assume that the approximate time position of the received preamble is to be known in advance, which may be achieved by adoption of a quasi-synchronous scheme such as slotted ALOHA system.

The transmitted base-band signal $s(k)$ in the data portion is expressed as

$$s(k) = d\sum_{n=0}^{L-1} c(n) e^{j\frac{2\pi}{L}nk}, 0 \le k \le L-1 \quad (1)$$

where $c(n)$ is the value for n-th chip of spreading sequence, and L is the number of samples per symbol with zero padding.

2.2. Symbol synchronizer

A circuit configuration for symbol synchronization is shown in Fig.3 [1]. In this circuit the received signal is demodulated with the locally generated orthogonal carriers and applied to a serial-to-parallel converter. The outputs from the serial-to-parallel converter are applied to an FFT circuit followed by a bank of phase shifters and correlation circuits (CC), each of which is performed with timing shifted by one chip time period. One of correlation circuits

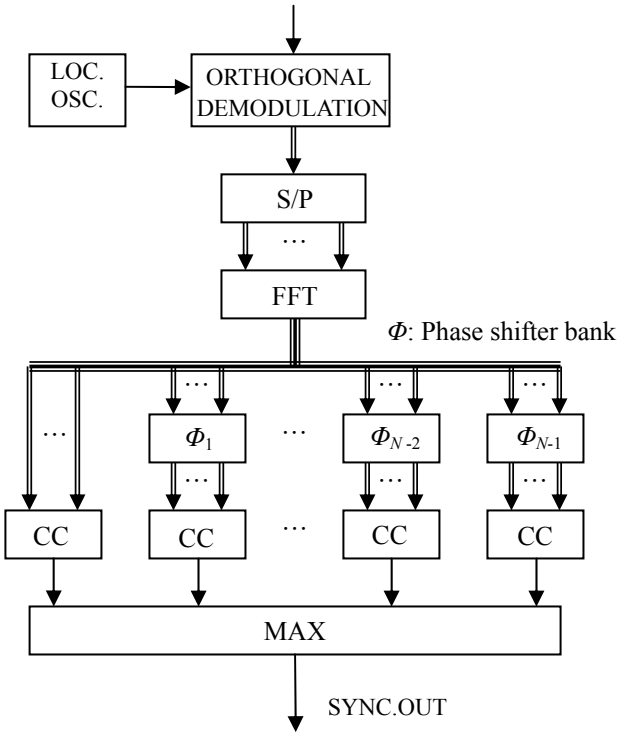


Fig.3. Symbol synchronizer

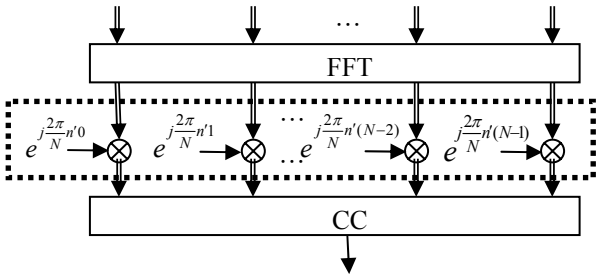


Fig.4. n'-th phase shifter bank $\Phi_{n'}$

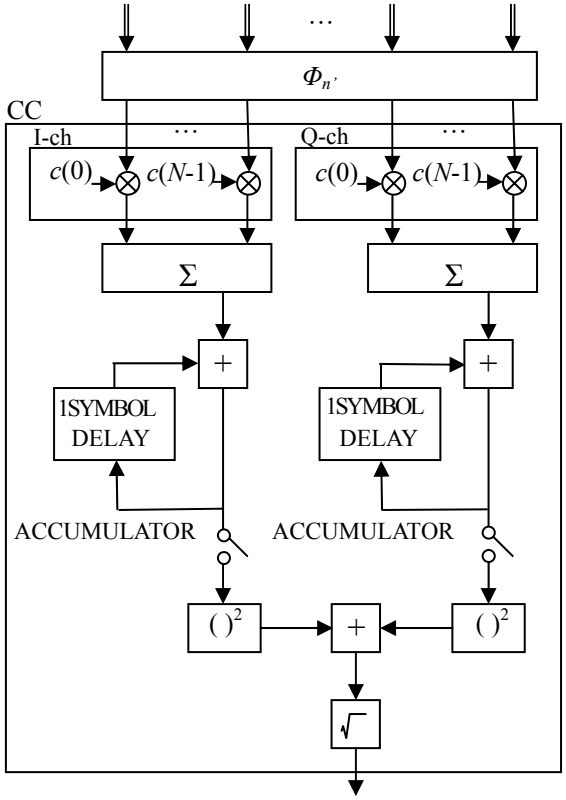


Fig.5. Correlation circuit

is illustrated in Fig.5. In this figure, the complex parallel outputs from the FFT circuit are applied to a pair of correlation circuits, each of which operates for either real (I-channel) or imaginary (Q-channel) component of the complex parallel outputs.

The output signal from the correlator is applied to an accumulator. The false detection probability can be reduced by this accumulation with repetition of several times. The outputs for I- and Q-channels are squared, respectively and added with each other. After passing through a square root circuit, the amplitude of signal is to be detected with sufficient signal-to-noise ratio.

The outputs from CC are compared with each other and

the maximum output is to be selected, and then applied to a decision circuit and decided as the correct synchronization timing.

In the proposed symbol synchronizer, N pairs of FFT and CC should have been prepared in order to achieve fast acquisition performance, but, the circuit configuration might become complicated. We considered, therefore, a simplified configuration in which (N-1) FFT circuits are replaced with the same number of phase shifters.

This is because n'-th FFT circuit ($FFT_{n'}$) is equivalent to a cyclic shift by n' chips from the timing of first FFT (FFT_0) since the preamble includes periodical pattern of multiple sequences as stated before, and the output of n'-th FFT circuit can be expressed as,

$$R_{n'}(n) = R_0(n)e^{j\frac{2\pi}{N}nn'} \tag{2}$$

where $R_0(n)$ represents the output of FFT in Fig.3, and is expressed as,

$$R_0(n) = \sum_{k=0}^{N-1} r(k)e^{-j\frac{2\pi}{N}kn} \tag{3}$$

where $r(k)$ represents the received base-band signal. The phase shifter $\Phi_{n'}$ shown in Fig.4 represents n'-th bank of phase shifters performing in parallel and expressed as,

$$\Phi_{n'} = \left\{ \phi_{n',0} = 0 \ , \ \phi_{n',1} = \frac{2\pi}{N}n' \right. \\ \left. ,\cdots, \ \phi_{n',N-1} = \frac{2\pi(N-1)}{N}n' \right\} \tag{4}$$
$$n' = 0,\cdots,(N-1)$$

where $\phi_{n'n}$ means n-th phase shifter in n'-th phase shifter bank.

The output from n'-th CC is expressed as follows;

$$F_{n'} = \sqrt{\left[F_{n'}^{I}\right]^2 + \left[F_{n'}^{Q}\right]^2} \tag{5}$$

$$F_{n'}^{I} = \sum_{l=0}^{M}\sum_{n=0}^{N-1}\left\{\mathrm{Re}\left[R_{n'+lN}(n)\right]c(n)\right\} \tag{6}$$

$$F_{n'}^{Q} = \sum_{l=0}^{M}\sum_{n=0}^{N-1}\left\{\mathrm{Im}\left[R_{n'+lN}(n)\right]c(n)\right\} \tag{7}$$

where the signal on I- and Q-channel represent real and imaginary components, respectively, and M is the number of accumulations.

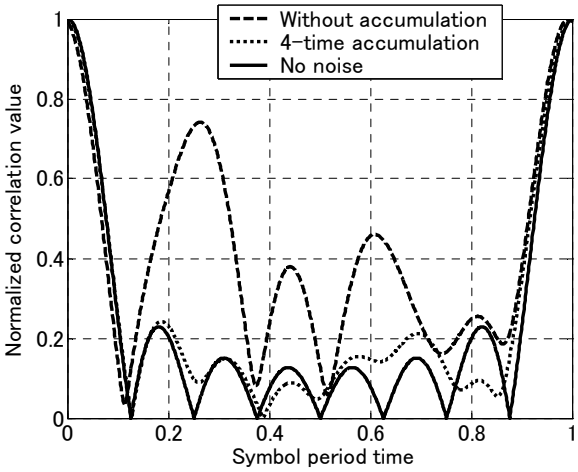


Fig.6. Example of $F_{n'}$

An example of $F_{n'}$ is shown in Fig.6. For E_S/N_0=15 [dB] with M=0 and 4, where E_S/N_0 represents the ratio of the symbol energy to the noise power spectral density. The correlated value is normalized by the maximum value. It is understood from Fig.6 that the correlated value increases as approaching the correct timing. In this figure, the characteristic without noise is also shown for comparison.

3. PERFORMANCE EVALUATION

At the output of selection circuit (MAX) in Fig.4, there is a possibility that a false selection, called false detection, would occur if some output of incorrect timing exceeded that of correct timing. In order to reduce the probability of false detection, the correlated outputs are accumulated several times.

The performance of the proposed synchronizer has been evaluated in terms of the probability of false detection through computer simulation with the parameters listed in Table 1 under additive white Gaussian noise (AWGN) and multi-path environment.

Table.1. Simulation parameters

Number of sub-carriers	8
Code pattern	{1,1,1,1,1,1,1,1}
Number of accumulation	0,2,4,6
Multipath model	2-path and 6-path

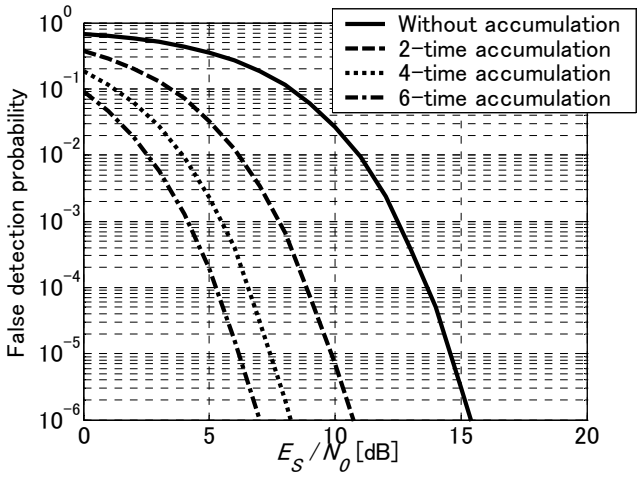


Fig.7. False detection probability versus E_S/N_0 without multi-path

3.1. Performance under AWGN environment

The evaluated false detection probabilities are shown in Fig.7 as a function of E_s/N_0 with the parameter of the number of times for the accumulations. It can be seen from this figure that the false detection probability decreases significantly as the number of accumulation increases. This improvement is considered to make up for a problem of increase in the length of the preamble portion.

3.2. Performance under multi-path environment

3.2.1. Performance under 2-path model

The multi-path model is set to be two-path for the evaluation. The evaluated false detection probabilities as a function of E_s/N_0 are shown in Fig.8 with the parameter of the number of times for the accumulations for the case where 5 [dB] of the desired signal-to-undesired signal ratio (*DUR*) and 3/16 [symbol period] of the time difference between two paths.

The false detection probability in this case increases remarkably compared with the case of AWGN shown in Fig.7. This increase is mainly caused by the detection of the signal coming through the delayed path. In other words, there are two peaks in the outputs from the correlation circuit, both of which may be regarded as correct timings in some cases. When we adopt a system that is not much affected by multi-path, such as a multi-carrier spread-spectrum (MC-SS) communication system [2], we can expect correct demodulation with either of synchronization timings. If the delay time of the delayed signal is within guard interval (GI) in usual OFDM systems, we may not have a serious problem in demodulating signals. If we regard, therefore, the delayed synchronization timing as correct one, the false detection probability may be reduced greatly.

It can be seen from Fig.7 and Fig.8 that the effectiveness of the accumulation under multi-path environment is almost the same as that under AWGN.

Figure 9 shows the false detection probability as a function of *DUR* with the parameters of the number of accumulations where E_S/N_0=10 [dB] and delay time difference=3/16 [symbol period] are set. The figure indicates that the false detection probability versus *DUR* decreases greatly as increase in the number of accumulations.

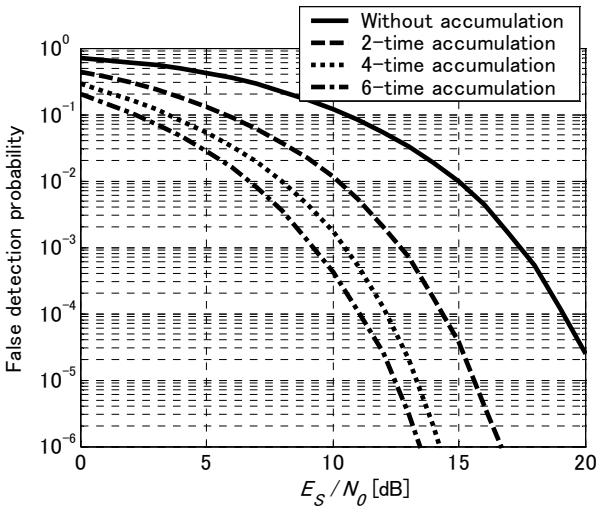


Fig.8. False detection probability versus E_S/N_0 with multi-path where *DUR*=5 [dB] and delay time difference=3/16 [symbol period]

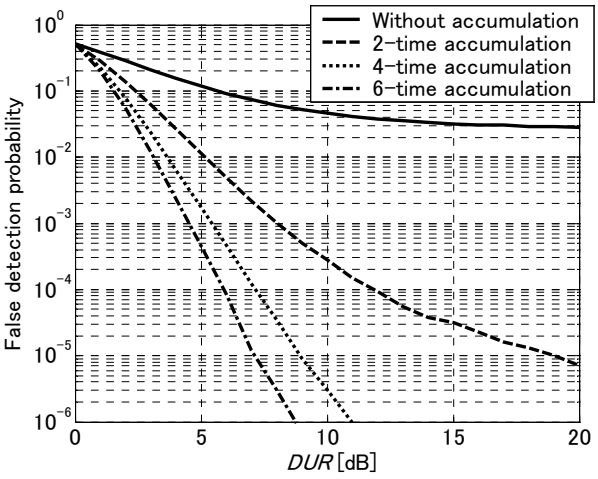


Fig.9. False detection probability versus *DUR* where E_S/N_0=10 [dB] and delay time difference=3/16 [symbol period]

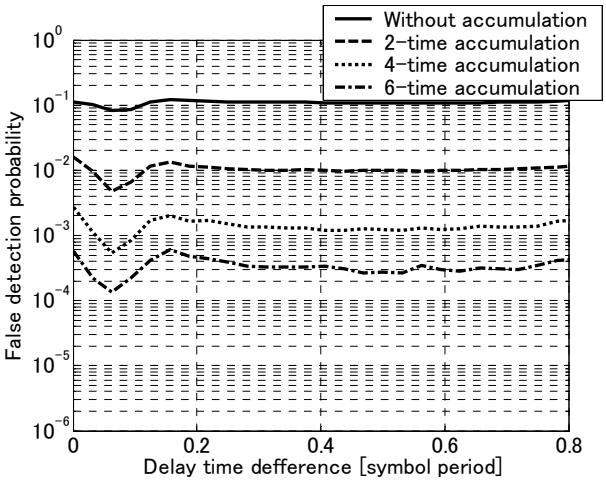
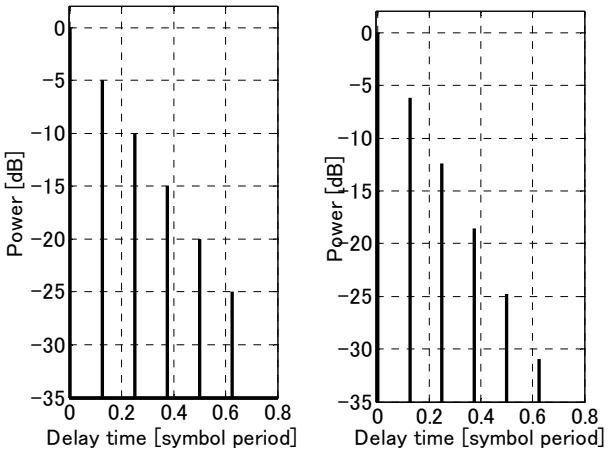


Fig.10. False detection probability versus delay time difference where E_S/N_0=10 [dB] and DUR=5 [dB]



(a) Model A (b) Model B

Fig.11. Six-path exponential multi-path model

Figure 10 shows the false detection probability as a function of delay time difference in symbol period with the parameters of the number of accumulations where E_S/N_0=10 [dB] and DUR=5 [dB] are set. It can be seen from Fig.10 that a false detection probability versus the delay time difference is almost constant throughout the symbol period.

3.2.2. Performance under 6-path model

In this subsection an effect of the number of multi-path is evaluated. The false detection probabilities are obtained under 6-path in which the levels of the paths decay exponentially with delay time. Two kinds of models for 6-path are considered as shown in Fig.11(a) and (b), respectively. These models have been arranged for comparison with the two-path model discussed before.

Model A shown in Fig.11(a) has been arranged so that the second path is set 5 [dB] lower than the first path and other paths decaying exponentially are added to evaluate these effects. The evaluated results are shown in Fig.12, in which a small amount of increase in the false detection probability is observed.

Model B shown in Fig.11(b) has been arranged so that the total power of the delayed paths have been adjusted to be 5dB down from the first path, so that the resulting second path is decreased by 6.2 [dB] and other paths decay exponentially. The evaluated results for this model are shown in Fig.13, in which the almost the same performance as that for the two-path model are obtained.

These two results indicate that the number of multi-paths will not give much influence to the performance.

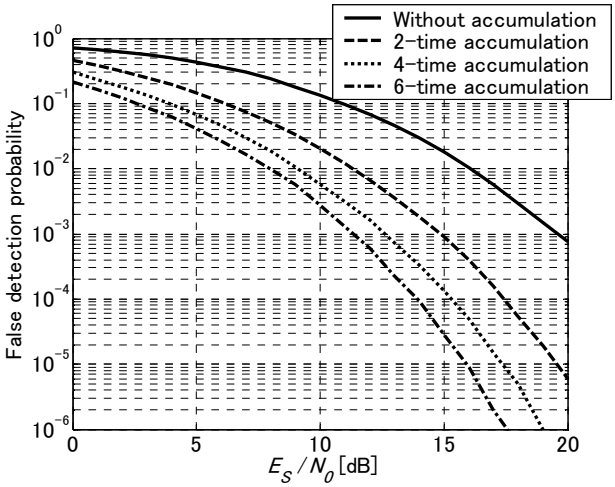


Fig.12. False detection probability versus E_S/N_0 (Model A)

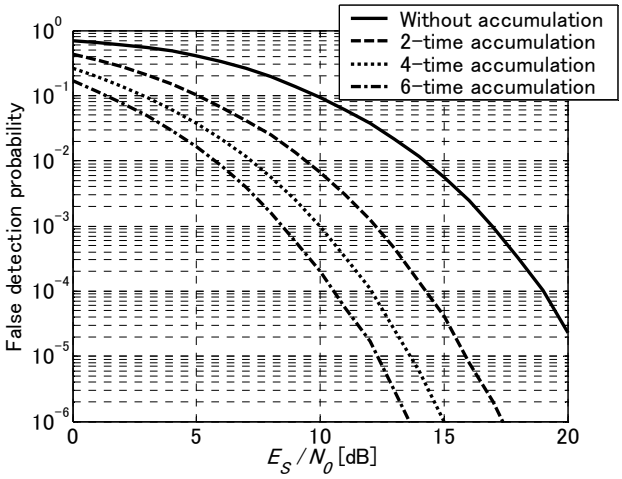


Fig.13. False detection probability versus E_S/N_0 (Model B)

4. CONCLUTION

We propose an improved symbol synchronizer for OFDM systems. In the proposed scheme, the synchronization is established through the processing which includes FFT, correlation, selection of the maximum correlated output and accumulation. The basic performance of the proposed synchronizer is evaluated in terms of the false detection probability in the presence of AWGN and multi-path assuming the packet transmission. It is shown that the proposed symbol synchronizer may provide the satisfied performance even under multi-path environment.

References

[1] S. Goto and A. Ogawa: “A Symbol Synchronizer for Multi-Carrier Spread-Spectrum Systems”, IEICE Trans. on Fundamentals, Vol.E-85-A, No.12, pp.2881-2885, Dec. 2002.

[2] K. Adachi and A. Ogawa: “Performance Characterization for MC-SS Packet Communications”, ISSSTA2004 (To be presented)

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Presented at ISITA 2004

Parma, Italy 10-13 October 2004

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Contents of the Presentation

1. Background and purpose of the study
2. Description of a proposed symbol synchronizer for wireless packet communication systems based on Multi-Carrier Spread Spectrum (MC-SS) scheme.
3. Performance of the symbol synchronizer
4. Conclusions

Background

✓**Demand**

- Broadband multimedia mobile communications
- Robustness against multi-path fading

Multi-carrier Packet Communication System

- OFDM (Orthogonal Frequency Division Multiplex)
- MC-SS (Multi-Carrier Spread-Spectrum)

Purpose

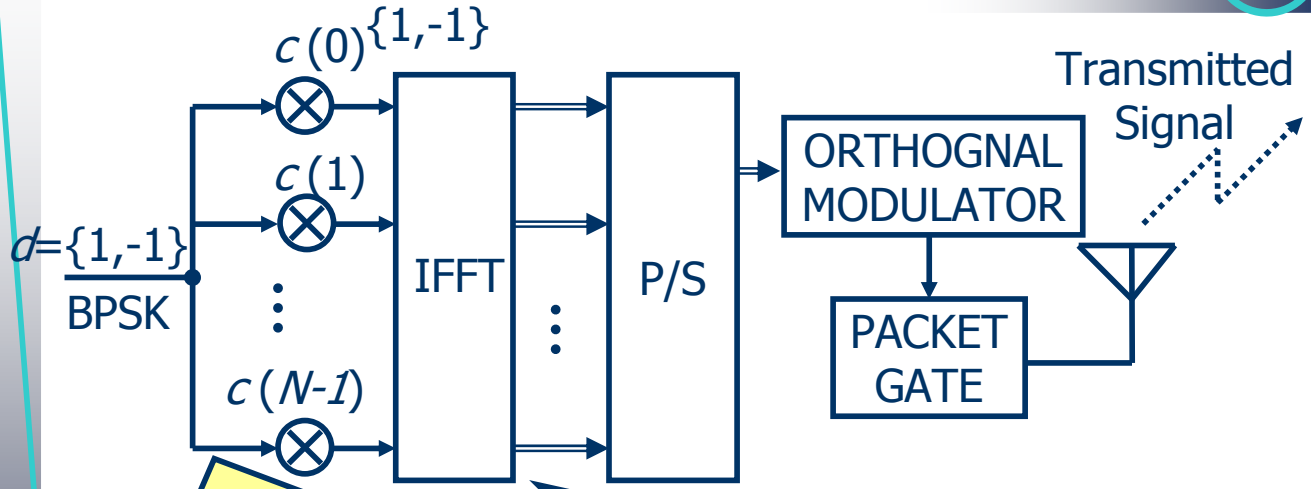
Problem

In the multi-carrier communication system, it is necessary to synchronize the timing for Fast Fourier Transform **(Symbol synchronization).**

Purpose of this research

To develop a simple and high-speed symbol synchronizer for wireless packet communication systems based on Multi-carrier Spread Spectrum (MC-SS).

Transmit Circuit for MC-SS system

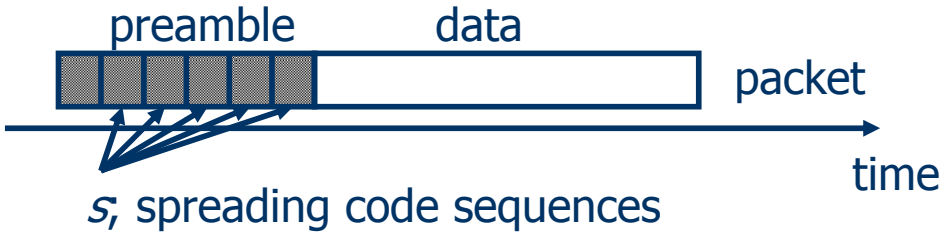


Binary input data
divided into N p
which are multipl
chips of spreading

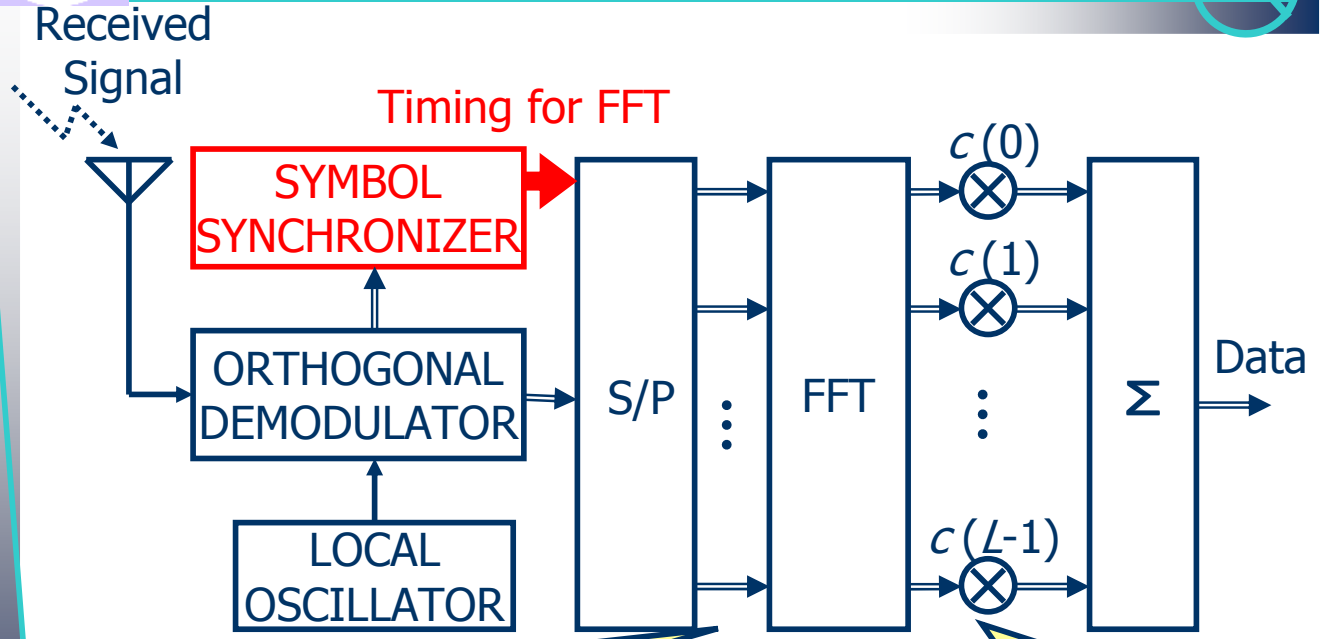
After this spreading process, Inverse Fast Fourier Transform is performed, and the output signals are applied to the parallel-to-serial converter.

Packet composition

- The preamble includes several spreading code sequences with the same pattern and is placed at the head of packet.
- The symbol synchronization is to be established within this preamble portion.



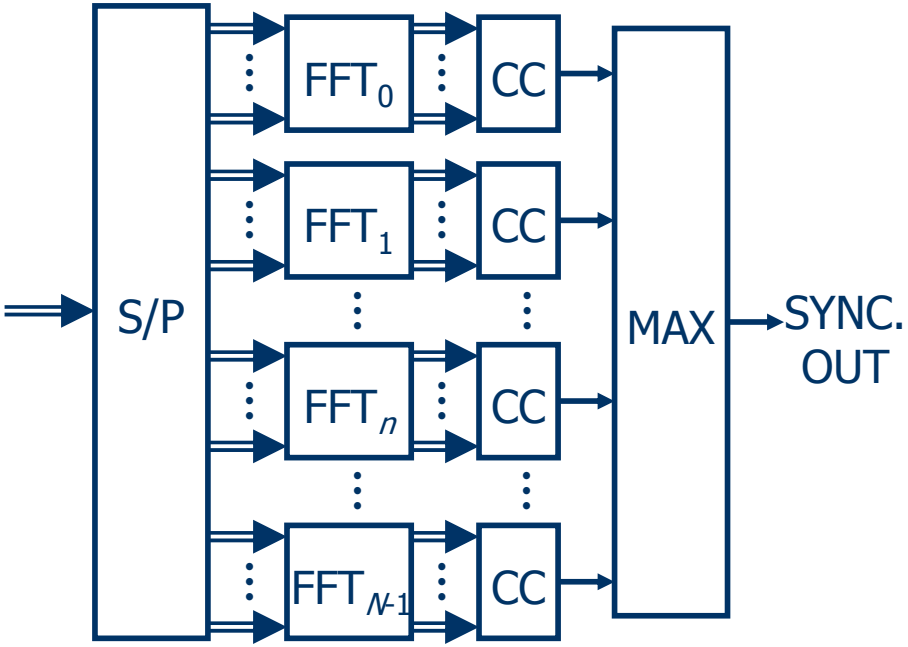
Receive Circuit for MC-SS system



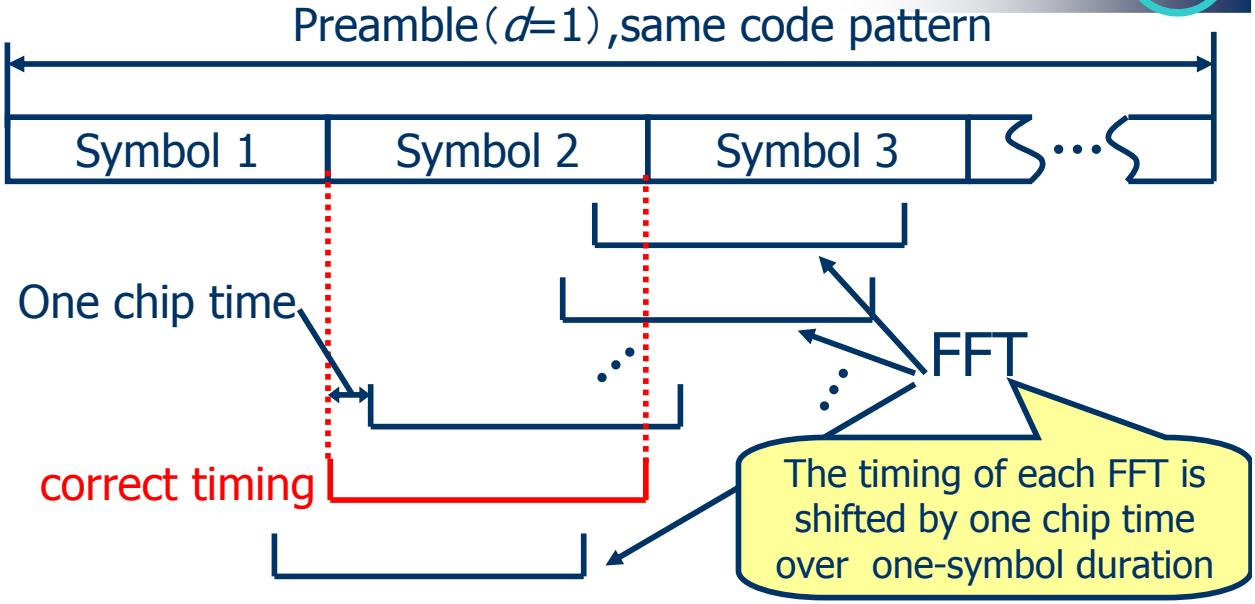
Serial-to-parallel converter and FFT are triggered according to the synchronization timing established with the symbol synchronizer.

The output signals are despread with the same spreading code as the transmitted one.

Symbol Synchronizer
(If N sets of FFT circuits were prepared.)



Detecting the correct timing for symbol synchronization



➢Correct timing for synchronization：
Timing with the largest correlated value

But, in this case we need many FFT circuits.

Reduction in the number of FFT

Instead of preparing many FFT circuits, these circuits can be replaced with a bank of phase shifters.

Output of n'-th FFT circuit (FFTn') can be expressed as,

$$R_{n'}(n) = R_0(n)\, e^{j\frac{2\pi}{N}nn'}$$

Phase Shifter Bank

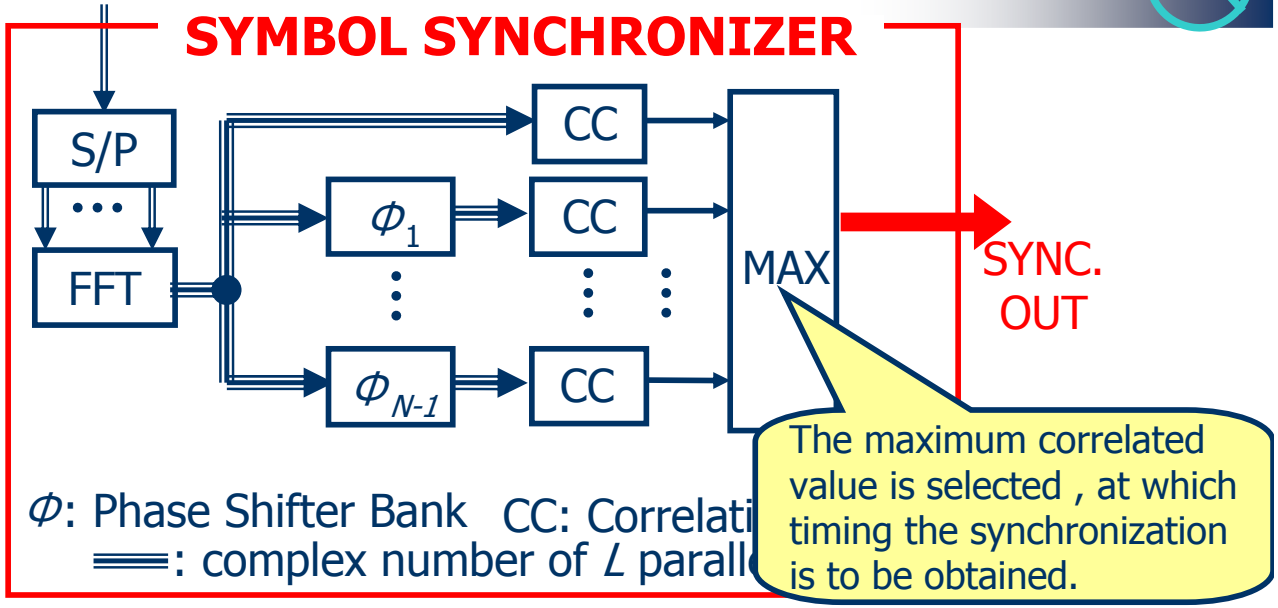
where $R_0(n)$ represents the output of first FFT, and expressed as;

$$R_0(n) = \sum_{k=0}^{N-1} r(k)\, e^{-j\frac{2\pi}{N}nk}$$

where $r(k)$ represents the received base-band signal

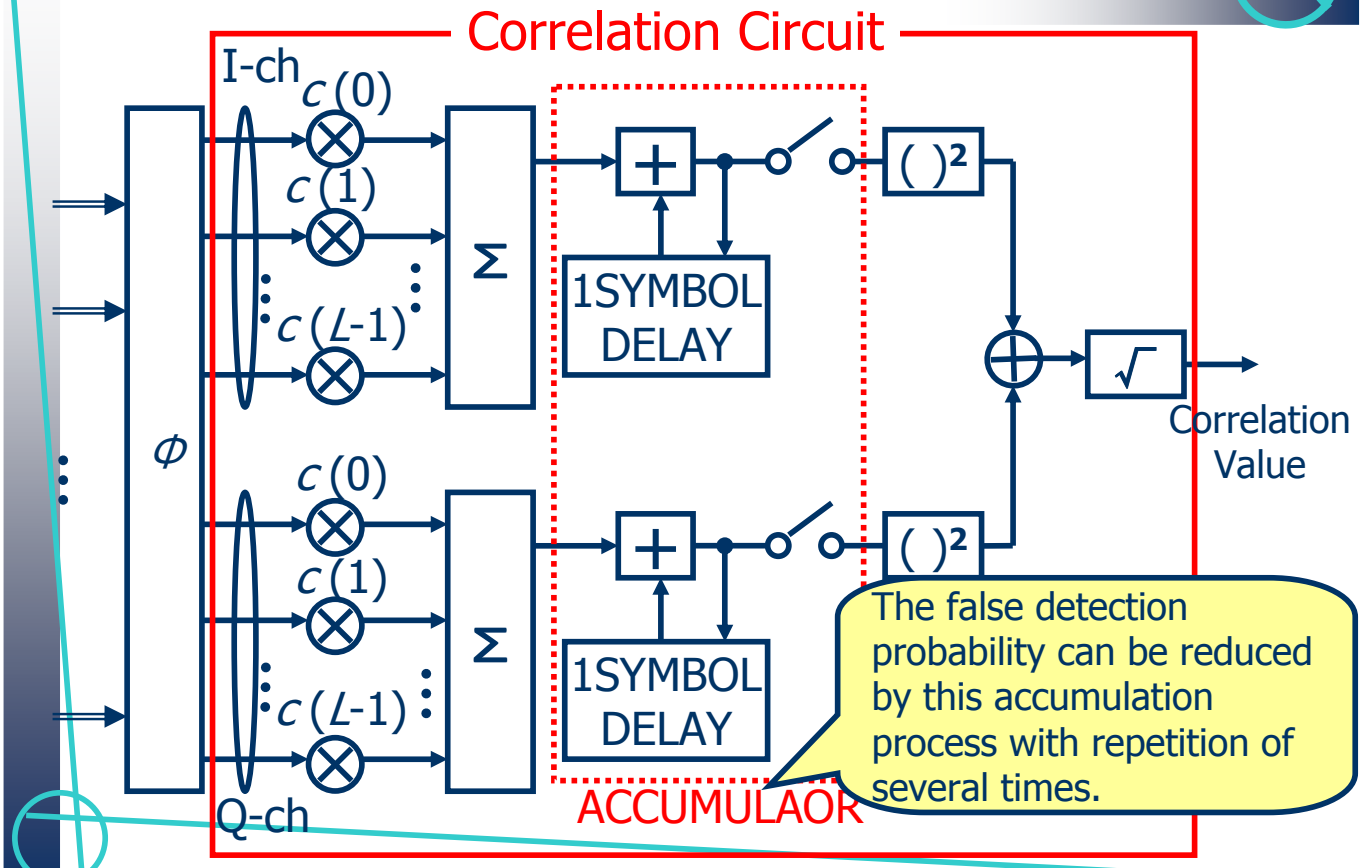
Thus, FFTn' is equivalent to n'-chip delay from the timing of first FFT circuit.

Simplified Symbol Synchronizer



N sets of FFT ⇒ One FFT + (*N*-1) sets of Phase Shifter Bank

Correlation Circuit



Accumulator

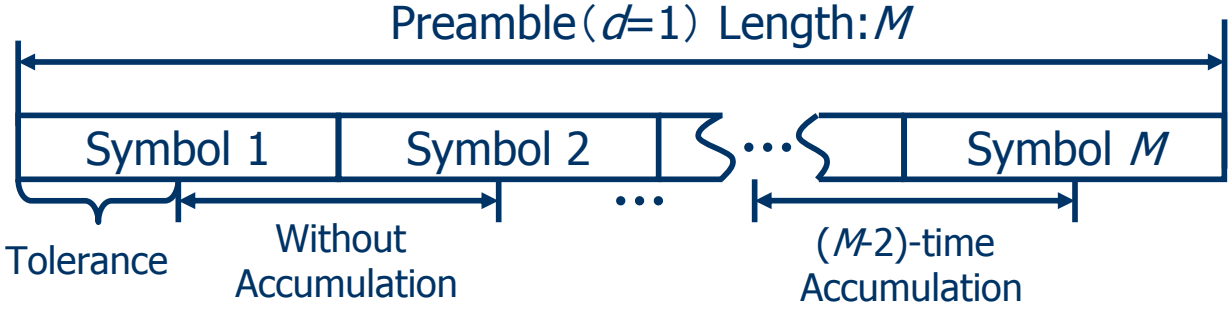
- When N-sets of FFT are applied, the synchronization process is made over the two-symbol period.
- On the other hand, in the case of phase shifter bank, the process will be made with one symbol period.

When we adopt the phase shifter bank, the correlated outputs may be uncorrelated with each other and the effect of the accumulation will become great as a result.

Accumulation and Preamble length

MAC：Slotted ALOHA

Tolerance: Assuming about 1 symbol period



The length of preamble portion can be estimated as the number of accumulation + 2 in symbols, assuming one symbol of error in arrival timing for the slotted ALOHA system.

Performance evaluation

- Under AWGN environment
  ⇒ False detection probability vs. *Es/No*
- Under Multi-path environment
  ⇒ False detection probability vs. *Es/No* and *DUR*

✓False detection

Some correlated outputs at the incorrect timings exceed that at the correct timing.

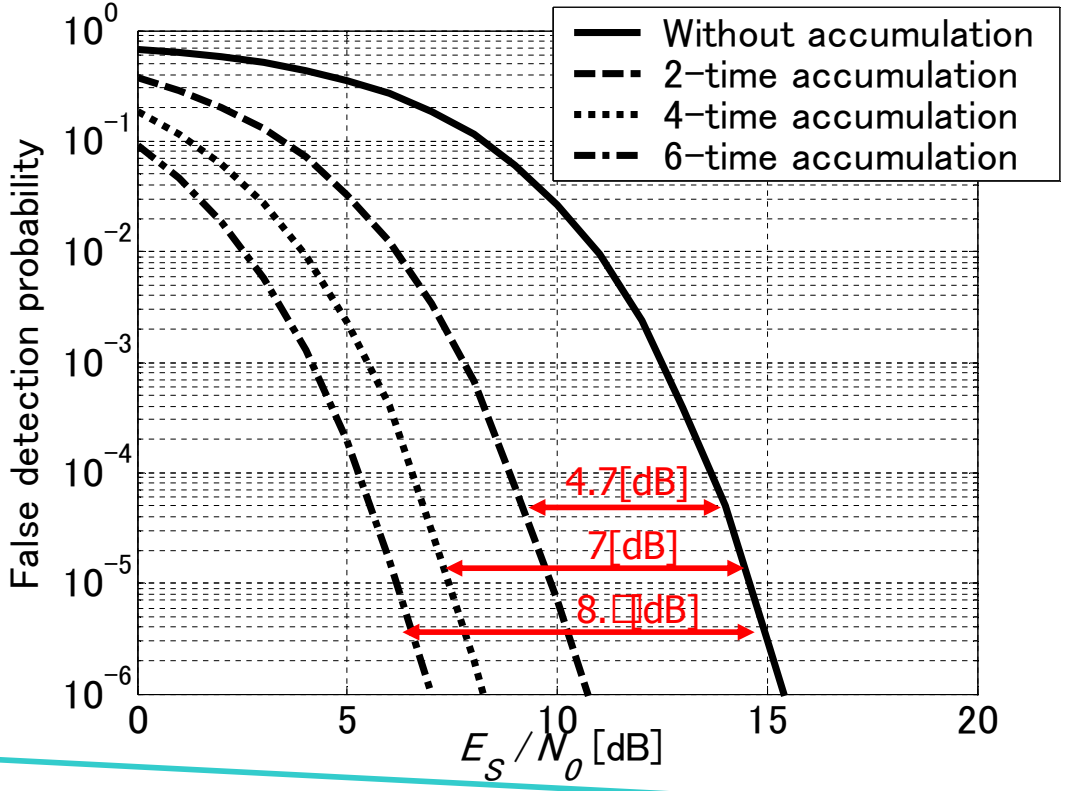
Simulation parameters

Simulation parameters

Number of sub-carriers	8
Code pattern	{1,1,1,1,1,1,1,1}
Sample per symbol	1024
Number of accumulation	0,2,4,6

Results (AWGN)

False detection probability vs. E_s/N_0



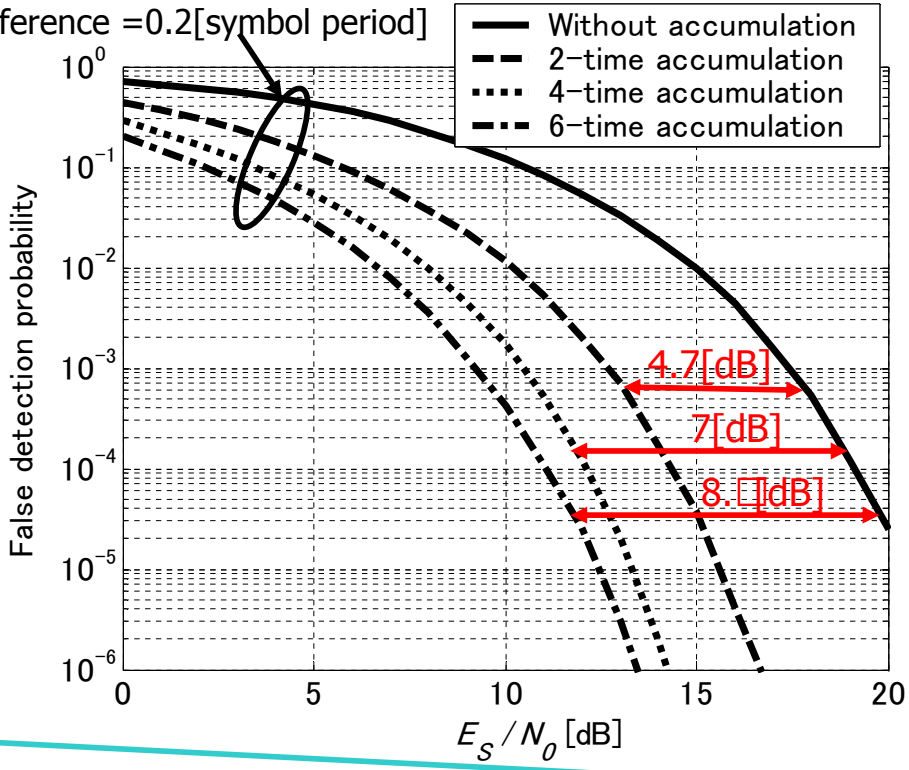
Results (Multi-path)

False detection probability vs. E_s/N_0

Number of path=2

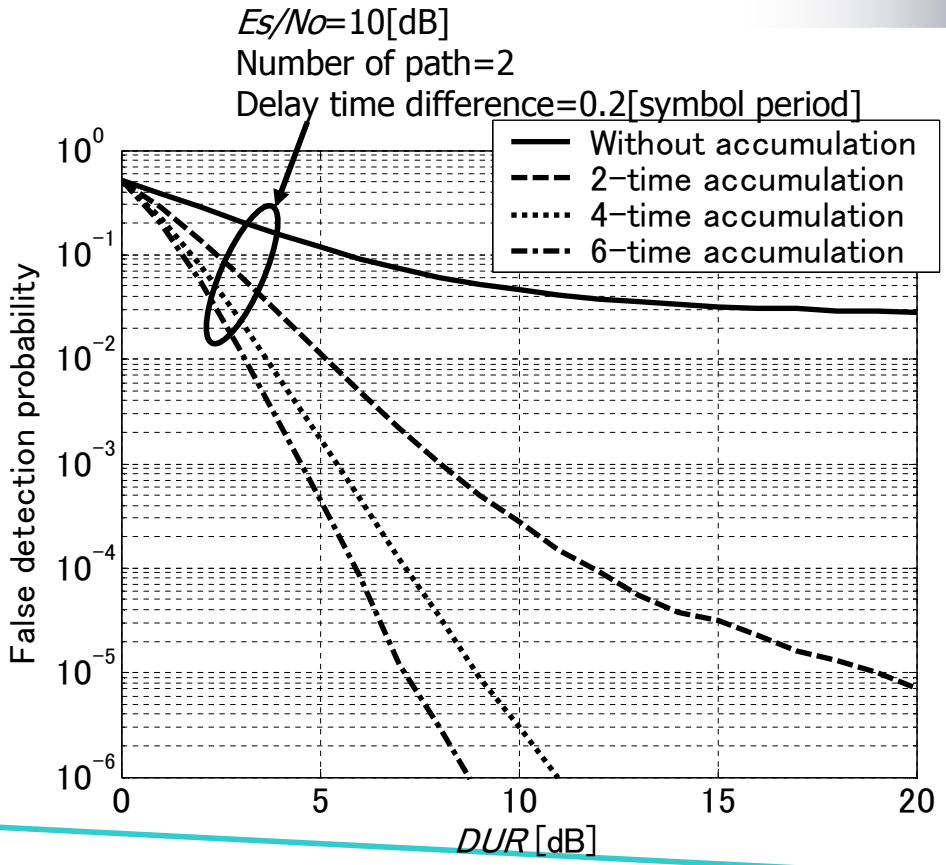
DUR=□[dB] *DUR* ; the ratio of desired to undesired signal level

Delay time difference =0.2[symbol period]



Results (Multi-path)

False detection probability vs. *DUR*



Conclusions

- We proposed an improved symbol synchronizer applicable to packet communications base on MC-SS scheme.
- In the proposed scheme, the synchronization is established through the processing which includes FFT, correlation, accumulation and selection of the maximum correlated output.
- With the accumulation process, a remarkable decrease in the false detection probability was achieved even under the multi-path environment.